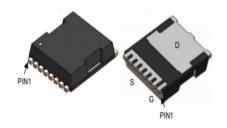
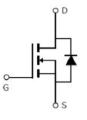


Main Product Characteristics:

V _{DSS}	100V		
R _{DS} (on)	1.4mΩ (typ.)		
I _D	351A		





TOLL

Schematic Diagram

Features and Benefits:

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150°C operating temperature



Description:

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute Max Rating:

Symbol	Parameter	Max.	Units	
In @ Tc = 25°C	Continuous Drain Current, Vos @ 10V ①	351		
In @ Tc = 100°C	Continuous Drain Current, Vos @ 10V ①	249	Α	
Ірм	Pulsed Drain Current ②	1406		
P _D @T _C = 25°C	Power Dissipation ③	429	W	
Vos	Drain-Source Voltage	100	V	
Vgs	Gate-to-Source Voltage	± 20	V	
Eas	Single Pulse Avalanche Energy @ L=0.5mH	1211	mJ	
TJ TSTG	Operating Junction and Storage Temperature Range	-55 to +175	°C	



Thermal Resistance

Symbol	Characterizes	Тур.	Max.	Units
Rejc	Junction-to-case ③	_	0.35	°C/W

Electrical Characteristics @TA=25°C unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
V(BR)DSS	Drain-to-Source breakdown voltage	100	_	_	V	Vgs = 0V, ID = 250µA
RDS(on)	Static Drain-to-Source on-resistance	_	1.4	2	mΩ	Vgs=10V,ID = 20A
V _{GS(th)}	Gate threshold voltage	2	_	4	V	V _{DS} = V _{GS} , I _D = 250µA
Ipss	Drain-to-Source leakage current	_	_	1	μA	V _{DS} = 100V,V _{GS} = 0V
l	Coto to Course forward lockers	_	_	100		V _{GS} =20V
lgss	Gate-to-Source forward leakage	_	_	-100	nA	V _{GS} = -20V
Ciss	Input capacitance	_	16400	_		V _{GS} = 0V
Coss	Output capacitance	_	2310	_	pF	V _{DS} = 50V
Crss	Reverse transfer capacitance	_	57	_		f = 1MHz
Qg	Total gate charge	_	135	_		I _D = 20A,
Qgs	Gate-to-Source charge	_	35	_	nC V _{DS} =50V,	V _{DS} =50V,
Qgd	Gate-to-Drain("Miller") charge	_	27	_		Vgs = 10V
td(on)	Turn-on delay time	_	65	_		
tr	Rise time	_	108	_		VGS=10V, VDD =50V,
td(off)	Turn-Off delay time	_	80	_	ns	R _{GEN} =3.6Ω,R _L =2.2Ω
tf	Fall time	_	23	_		

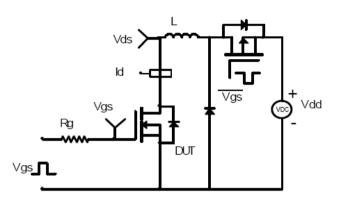
Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
ls	Continuous Source Current (Body Diode)	_	_	351	А	MOSFET symbol showing the
Ism	Pulsed Source Current (Body Diode)	_	_	1406	Α	integral reverse p-n junction diode.
V _{SD}	Diode Forward Voltage	_	_	1.2	V	Is=2A, Vgs=0V
trr	Reverse Recovery Time	_	85	_	ns	T _J = 25°C, I _F =20A, di/dt =
Qrr	Reverse Recovery Charge	_	251	_	nC	100A/μs

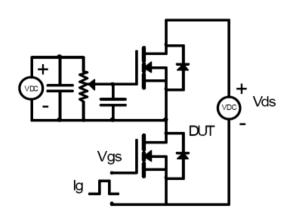


Test Circuits and Waveforms

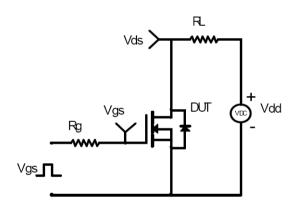
EAS Test Circuit:



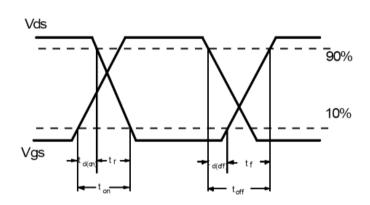
Gate Charge Test Circuit:



Switching Time Test Circuit:



Switching Waveforms:



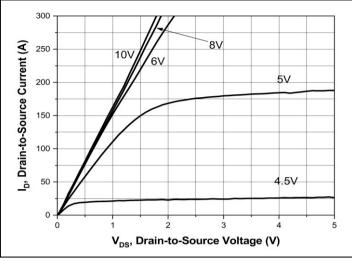
Version: 1.0

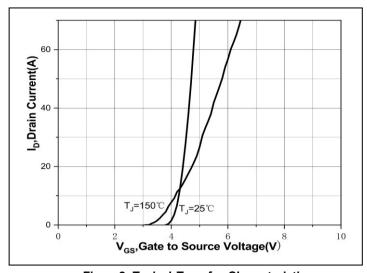
Notes:

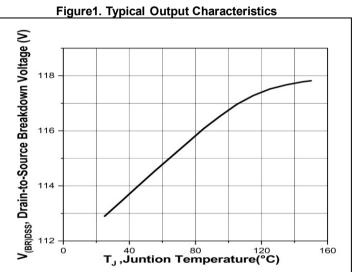
- ①Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- (3) The power dissipation P_D is based on max. junction temperature, using junction-to-case thermal resistance.



Typical Electrical and Thermal Characteristics







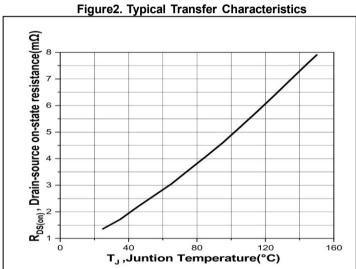
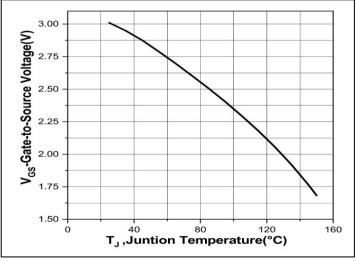


Figure 3. Drain-to-Source Breakdown Voltage vs. Junction
Temperature

Figure4. Normalized On-Resistance vs. Junction Temperature



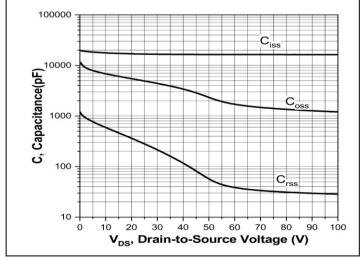


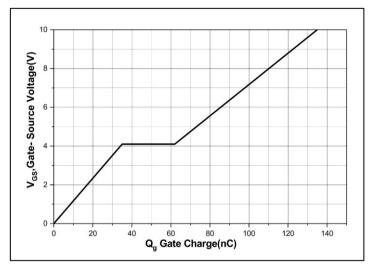
Figure 5. Normalized V_{GS}(th) vs. Junction Temperature

Figure 6. Capacitance Characteristics





Typical Electrical and Thermal Characteristics



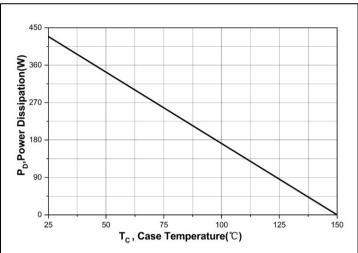


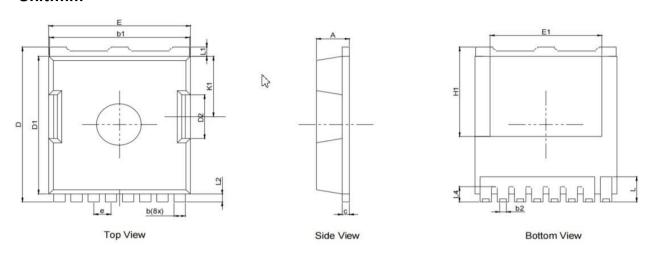
Figure7. Gate Charge

Figure8. Power Dissipation



Mechanical Data:

Unit:mm



DIM	MILLIMETER				
DIM.	MIN. NOM.		MAX.		
Α	2.20	2.30	2.40		
b	0.70	0.80	0.90		
b1	9.65	9.80	9.95		
С	0.40	0.50	0.60		
D	11.48	11.48 11.68			
D1	10.28		10.70		
D2	3.30				
E	9.70	10.10			
E1	8.10				
е	1.20 (BSC)				
H1	6.70	7.30			
K1	4.55				
L	1.35		2.10		
L1	0.70				
L2	0.60				
L4	0.95	1.20	1.35		





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