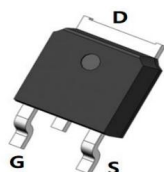
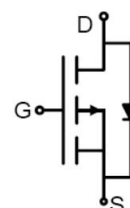


Main Product Characteristics:

V_{DSS}	-20V
$R_{DS(on)}$	5m Ω (typ.)
I_D	-60A


TO-252

Schematic Diagram
Features and Benefits:

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150°C operating temperature


Description:

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute Max Rating:

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ ①	-60	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ ①	-39	
I_{DM}	Pulsed Drain Current ②	-240	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation ③	60	W
V_{DS}	Drain-Source Voltage	-20	V
V_{GS}	Gate-to-Source Voltage	± 12	V
E_{AS}	Single Pulse Avalanche Energy @ $L=0.5\text{mH}$	40	mJ
$T_J \quad T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +150	$^\circ\text{C}$

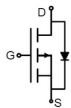
Thermal Resistance

Symbol	Characterizes	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ③	—	2.1	$^{\circ}\text{C}/\text{W}$

Electrical Characterizes @ $T_A=25^{\circ}\text{C}$ unless otherwise specified

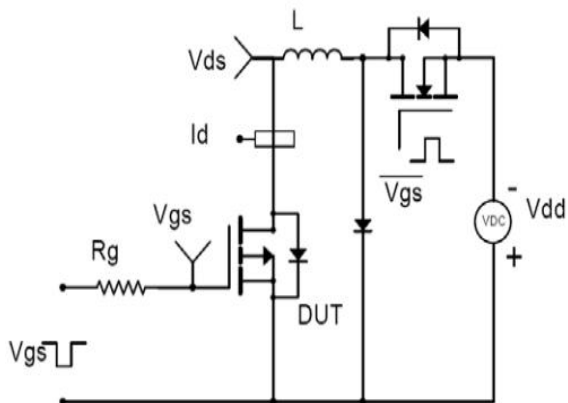
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	-20	—	—	V	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	5	6.5	m Ω	$V_{GS} = -4.5\text{V}, I_D = -15\text{A}$
		—	7	9		$V_{GS} = -2.5\text{V}, I_D = -12\text{A}$
$V_{GS(th)}$	Gate threshold voltage	-0.4	—	-1	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
I_{DSS}	Drain-to-Source leakage current	—	—	-1	μA	$V_{DS} = -20\text{V}, V_{GS} = 0\text{V}$
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 12\text{V}$
		—	—	-100		$V_{GS} = -12\text{V}$
C_{iss}	Input capacitance	—	3460	—	pF	$V_{GS} = 0\text{V}$
C_{oss}	Output capacitance	—	545	—		$V_{DS} = -10\text{V}$
C_{rss}	Reverse transfer capacitance	—	490	—		$f = 1\text{MHz}$
Q_g	Total gate charge	—	55	—	nC	$I_D = -15\text{A},$
Q_{gs}	Gate-to-Source charge	—	8	—		$V_{DS} = -4.5\text{V},$
Q_{gd}	Gate-to-Drain("Miller") charge	—	15	—		$V_{GS} = -4.5\text{V}$
$t_{d(on)}$	Turn-on delay time	—	10	—	ns	$V_{GS} = -10\text{V}, V_{DD} = -10\text{V},$ $R_{GEN} = 2.7\Omega, I_D = -13\text{A}$
t_r	Rise time	—	110	—		
$t_{d(off)}$	Turn-Off delay time	—	155	—		
t_f	Fall time	—	160	—		

Source-Drain Ratings and Characteristics

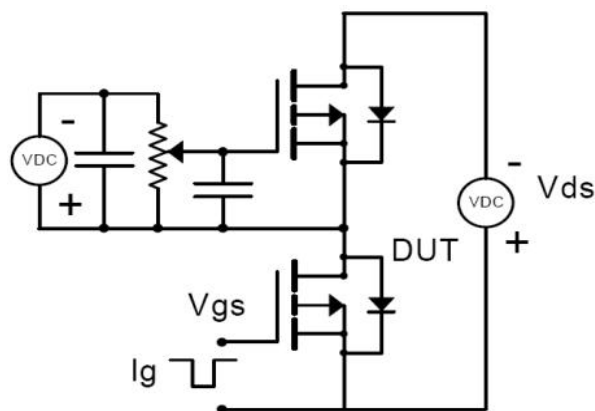
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-60	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	-240	A	
V_{SD}	Diode Forward Voltage	—	—	-1.2	V	$I_S = -30\text{A}, V_{GS} = 0\text{V}$
t_{rr}	Reverse Recovery Time	—	18	—	ns	$T_J = 25^{\circ}\text{C}, I_F = -15\text{A}, di/dt = 100\text{A}/\mu\text{s}$
Q_{rr}	Reverse Recovery Charge	—	7.7	—	nC	

Test Circuits and Waveforms

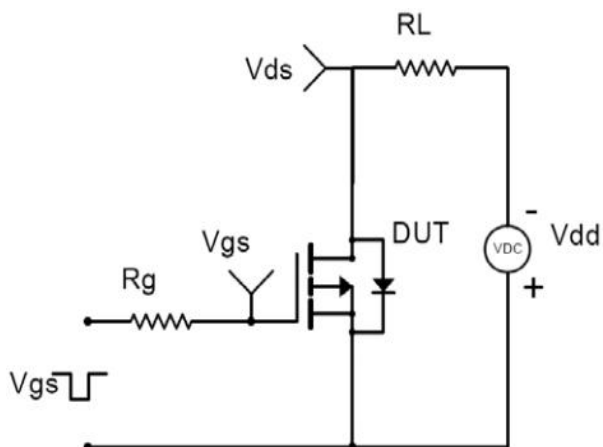
EAS Test Circuit:



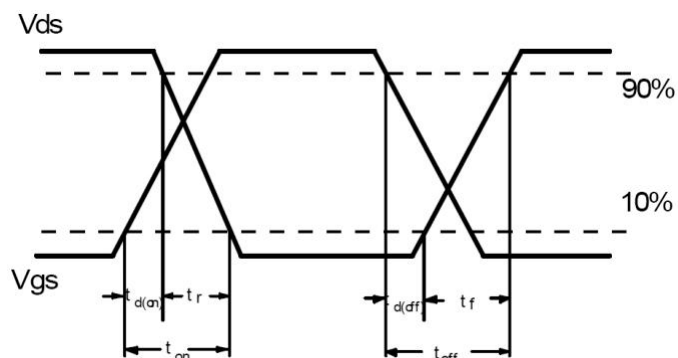
Gate Charge Test Circuit:



Switching Time Test Circuit:



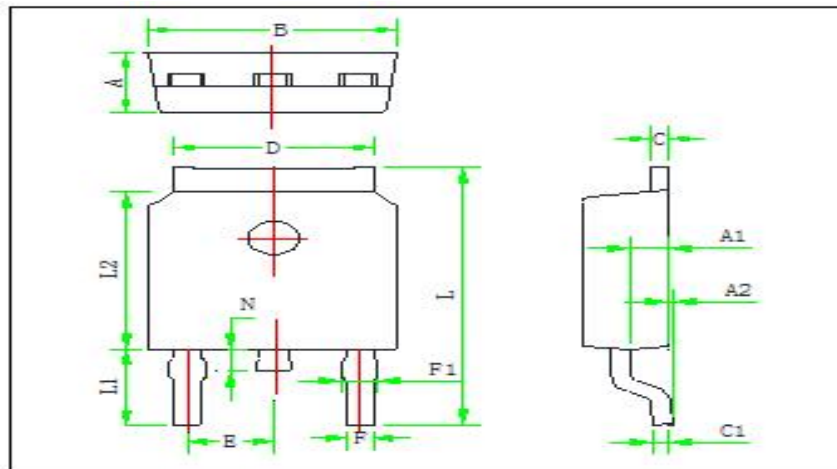
Switching Waveforms:



Notes:

- ① Calculated continuous current based on maximum allowable junction temperature.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.

Mechanical Data:



Symbol	Min	Typ	Max
A	2.20	2.30	2.40
A1	0.91	1.01	1.11
A2	0.05	0.15	0.25
B	6.45	6.60	6.75
C	0.45	0.50	0.58
C1	0.45	0.50	0.58
D	5.12	5.32	5.52
E	2.286 TYP		
F	0.66	0.76	0.86
F1	0.66	0.86	1.06
L	9.60	9.90	10.20
L1	2.6	2.8	3.0
L2	5.95	6.10	6.25
N	0.60	0.80	1.00

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