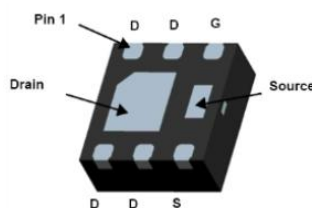
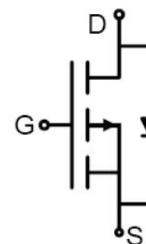


Main Product Characteristics:

V_{DSS}	-12V
$R_{DS(on)}$	13.2m Ω (typ.)
I_D	-11.5A


DFN2x2-6L

Schematic Diagram
Features and Benefits:

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150°C operating temperature


Description:

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute Max Rating:

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ ①	-11.5	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ ①	-7.3	
I_{DM}	Pulsed Drain Current ②	-46	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation ③	3	W
V_{DS}	Drain-Source Voltage	-12	V
V_{GS}	Gate-to-Source Voltage	± 10	V
$T_J \quad T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +150	$^\circ\text{C}$

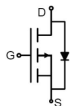
Thermal Resistance

Symbol	Characterizes	Typ.	Max.	Units
R _{θJA}	Junction-to-ambient (t ≤ 10s) ④	—	40	°C/W

Electrical Characteristics @T_A=25°C unless otherwise specified

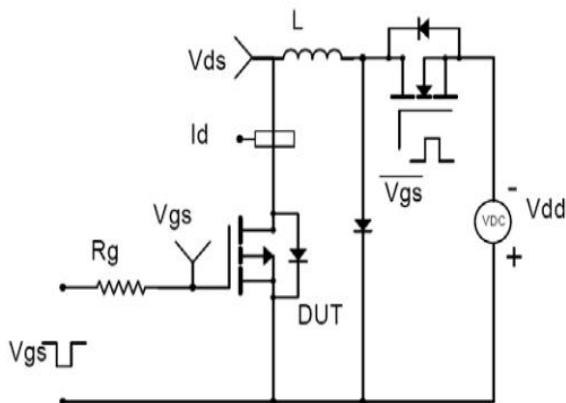
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source breakdown voltage	-12	—	—	V	V _{GS} = 0V, I _D = -250μA
R _{DS(on)}	Static Drain-to-Source on-resistance	—	13.2	17.2	mΩ	V _{GS} = -4.5V, I _D = -5A
		—	19.6	26		V _{GS} = -2.5V, I _D = -4A
V _{GS(th)}	Gate threshold voltage	-0.5	—	-1	V	V _{DS} = V _{GS} , I _D = -250μA
I _{DSS}	Drain-to-Source leakage current	—	—	-1	μA	V _{DS} = -12V, V _{GS} = 0V
I _{GSS}	Gate-to-Source forward leakage	—	—	100	nA	V _{GS} = 10V
		—	—	-100		V _{GS} = -10V
C _{iss}	Input capacitance	—	1450	—	pF	V _{GS} = 0V
C _{oss}	Output capacitance	—	324	—		V _{DS} = -10V
C _{rss}	Reverse transfer capacitance	—	283	—		f = 1MHz
Q _g	Total gate charge	—	16	—	nC	I _D = -5A,
Q _{gs}	Gate-to-Source charge	—	3.5	—		V _{DS} = -10V,
Q _{gd}	Gate-to-Drain("Miller") charge	—	4.1	—		V _{GS} = -4.5V
t _{d(on)}	Turn-on delay time	—	16	—	ns	V _{GS} = -4.5V, V _{DS} = -10V, R _{GEN} = 3Ω, R _L = 2Ω
t _r	Rise time	—	65	—		
t _{d(off)}	Turn-Off delay time	—	70	—		
t _f	Fall time	—	62	—		

Source-Drain Ratings and Characteristics

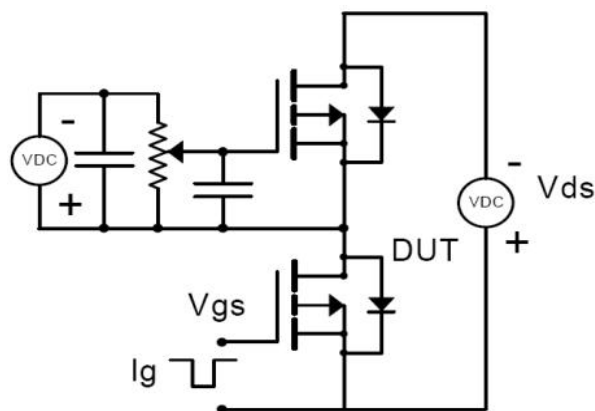
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-11.5	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode)	—	—	-46	A	
V _{SD}	Diode Forward Voltage	—	—	-1.2	V	I _S = -5A, V _{GS} = 0V

Test Circuits and Waveforms

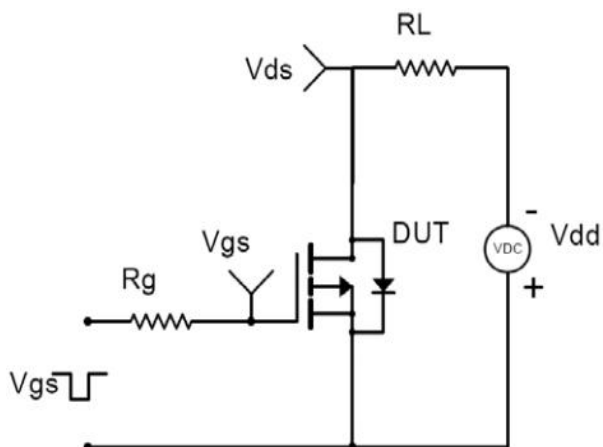
EAS Test Circuit:



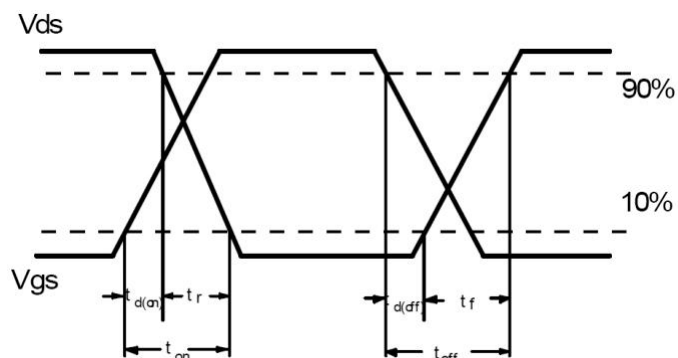
Gate Charge Test Circuit:



Switching Time Test Circuit:



Switching Waveforms:

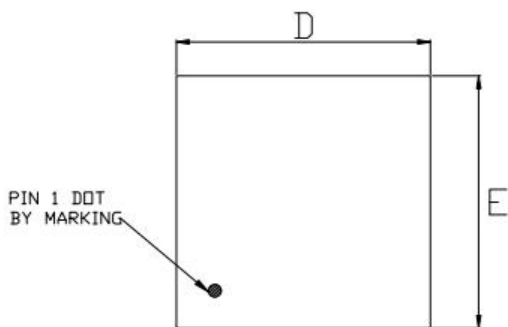


Notes:

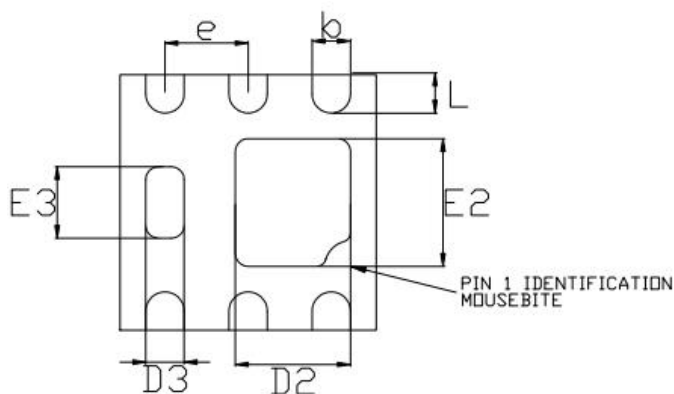
- ① Calculated continuous current based on maximum allowable junction temperature.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation P_D is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$

Mechanical Data:

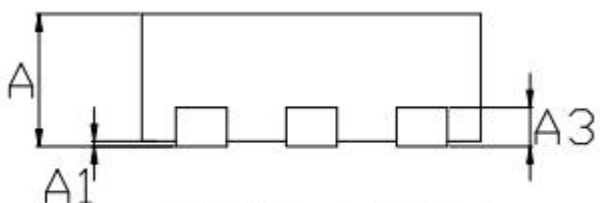
DFN 2 x 2-6L PACKAGE INFORMATION



TOP VIEW



BOTTOM VIEW



SIDE VIEW

COMMON DIMENSIONS(MM)			
PKG.	W:VERY VERY THIN		
REF.	MIN.	NOM.	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.20 REF.		
D	1.95	2.00	2.05
E	1.95	2.00	2.05
D2	0.85	0.90	0.95
E2	0.95	1.00	1.05
D3	0.25	0.30	0.35
E3	0.51	0.56	0.61
b	0.25	0.30	0.35
L	0.25	0.30	0.35
e	0.65 BSC		

Notes:

①Dimensions are in millimeters.

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