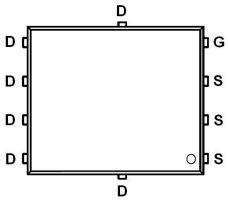
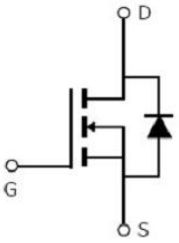
Main Product Characteristics:

V_{DSS}	60V
R_{DS}(on)	1.9mΩ (typ.)
I_D	200A

PDFN5x6-8L



Pin Assignments



Schematic Diagram

Features and Benefits:

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150℃ operating temperature

RoHS Compliant

Description:

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute Max Rating:

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V ①	200	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V ①	160	
I_{DM}	Pulsed Drain Current ②	800	
P_D @T_C = 25°C	Power Dissipation ③	156	W
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy @ L=0.5mH	306	mJ
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C

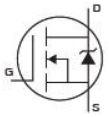
Thermal Resistance

Symbol	Characterizes	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ③	—	0.8	℃/W
$R_{\theta JA}$	Junction-to-ambient (t ≤ 10s) ④	—	42	℃/W

Electrical Characterizes @T_A=25℃ unless otherwise specified

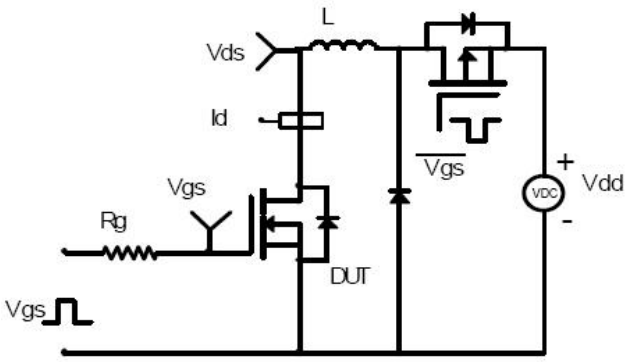
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	60	—	—	V	V_{GS} = 0V, I_D = 250μA
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	1.9	2.5	mΩ	V_{GS}=10V,I_D = 30A
		—	2.6	3.4		V_{GS}=4.5V,I_D = 20A
$V_{GS(th)}$	Gate threshold voltage	1	—	2.5	V	V_{DS} = V_{GS}, I_D = 250μA
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	V_{DS} = 60V,V_{GS} = 0V
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	V_{GS} =20V
		—	—	-100		V_{GS} = -20V
C_{iss}	Input capacitance	—	5440	—	pF	V_{GS} = 0V
C_{oss}	Output capacitance	—	2200	—		V_{DS} = 25V
C_{rss}	Reverse transfer capacitance	—	135	—		f = 1MHz
Q_g	Total gate charge	—	100	—	nC	I_D = 30A,
Q_{gs}	Gate-to-Source charge	—	15	—		V_{DS}=30V,
Q_{gd}	Gate-to-Drain("Miller") charge	—	20	—		V_{GS} = 10V
$t_{d(on)}$	Turn-on delay time	—	15	—	ns	V_{GS}=10V, V_{DD} =30V, R_{GEN}=3Ω,I_D =30A
t_r	Rise time	—	38	—		
$t_{d(off)}$	Turn-Off delay time	—	75	—		
t_f	Fall time	—	95	—		

Source-Drain Ratings and Characteristics

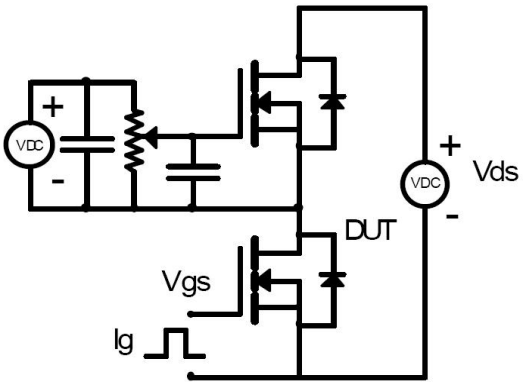
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	200	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	800	A	
V_{SD}	Diode Forward Voltage	—	—	1.2	V	I_S=30A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	—	54	—	ns	T_J = 25°C, I_F =30A, di/dt = 100A/μs
Q_{rr}	Reverse Recovery Charge	—	60	—	nC	

Test Circuits and Waveforms

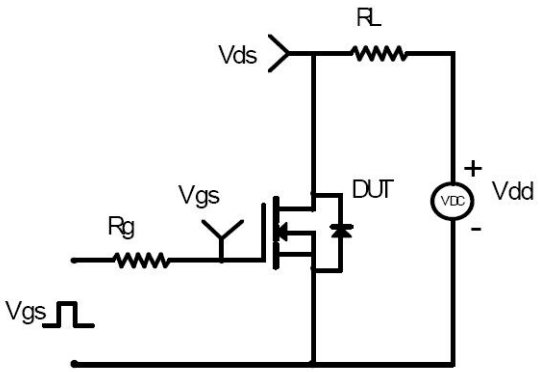
EAS Test Circuit:



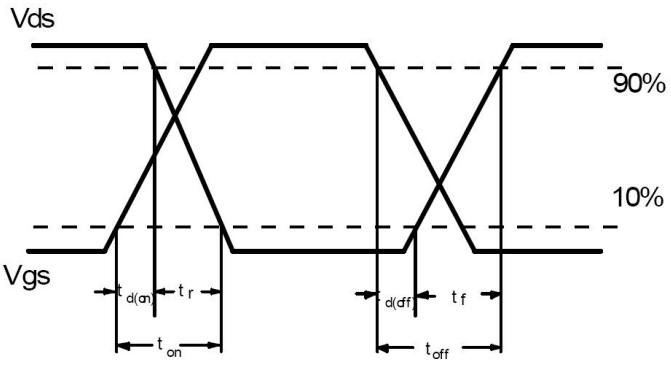
Gate Charge Test Circuit:



Switching Time Test Circuit:



Switching Waveforms:



Notes:

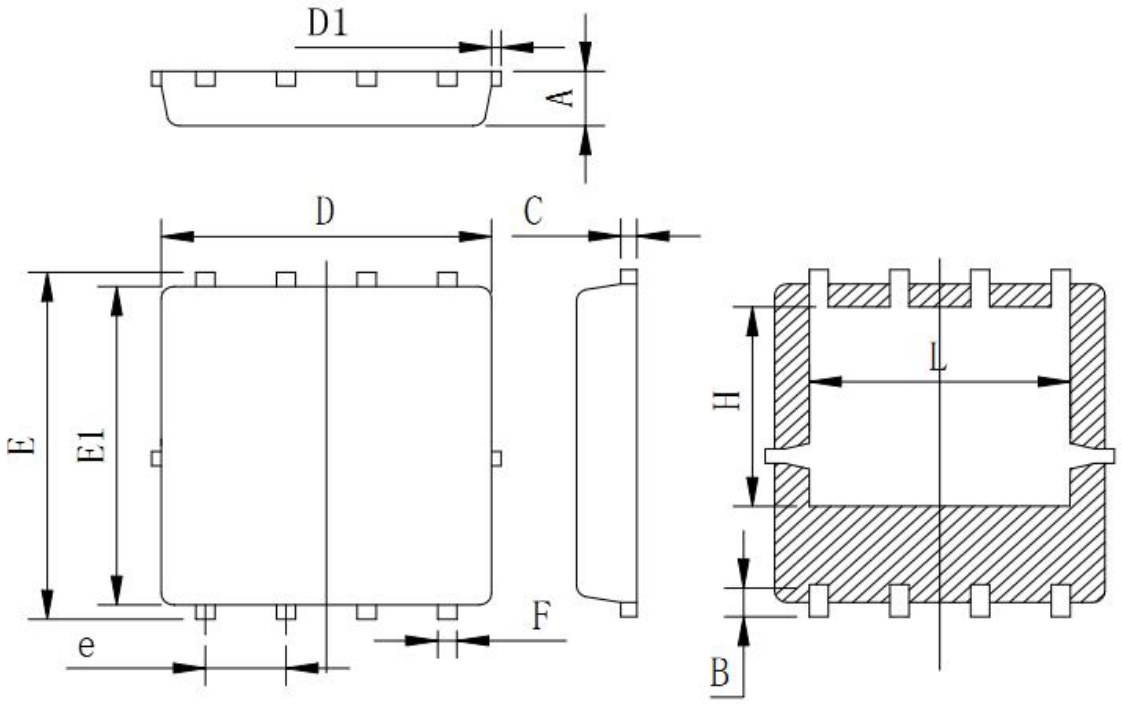
①Calculated continuous current based on maximum allowable junction temperature.

②Repetitive rating; pulse width limited by max. junction temperature.

③The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.

④The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C

Mechanical Data：



Symbol	Min	Typ	Max
A	0.90	0.95	1.00
B	0.48	0.58	0.68
C	0.20	0.254	0.30
D	5.00	5.20	5.40
D1			0.15
E	5.90	6.05	6.20
E1	5.40	5.55	5.70
e	1.22	1.27	1.32
F	0.25	0.30	0.35
H	3.27	3.47	3.67
L	3.80	4.00	4.20

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