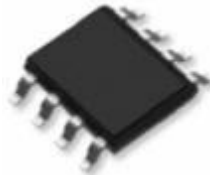
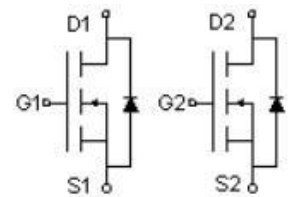


Main Product Characteristics:

V_{DSS}	60V
$R_{DS(on)}$	65m Ω (typ.)
I_D	3.5A ①


SOP-8

Marking and Pin Assignments

Schematic Diagram
Features and Benefits:

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150°C operating temperature


Description:

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute Max Rating:

Symbol	Parameter	Max.	Units
I_D @ $T_A = 25^\circ\text{C}$	Continuous Drain Current ①	3.5	A
I_D @ $T_A = 70^\circ\text{C}$	Continuous Drain Current ①	2.8	
I_{DM}	Pulsed Drain Current ②	20	
P_D @ $T_A = 25^\circ\text{C}$	Power Dissipation ③	2.4	W
V_{DS}	Drain- Source Voltage	60	V
V_{GS}	Gate- to- Source Voltage	± 25	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Resistance

Symbol	Characterizes	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-ambient ($t \leq 10s$) ④	—	62.5	C/ W

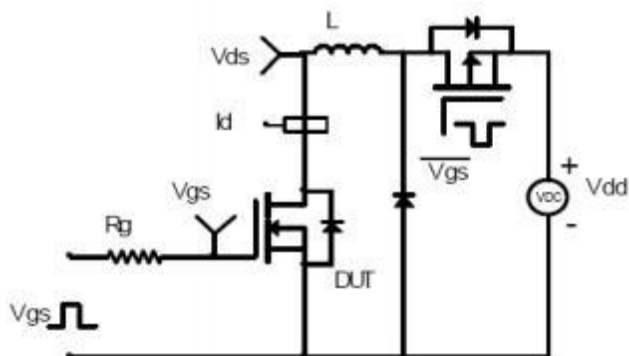
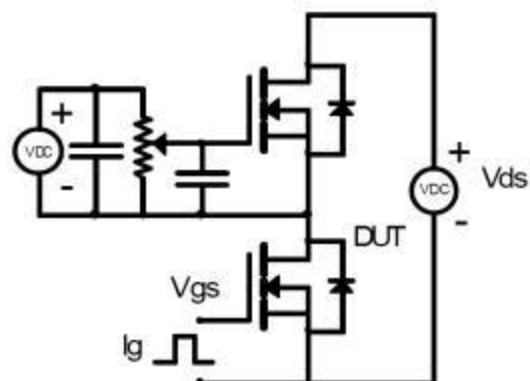
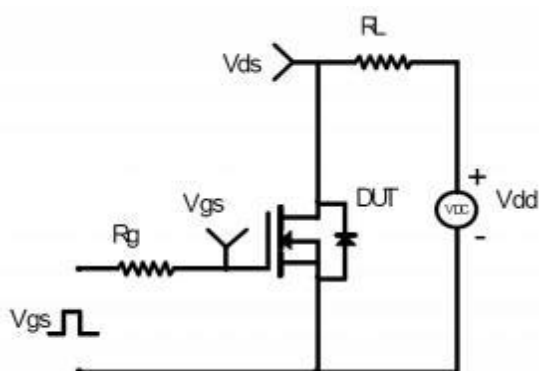
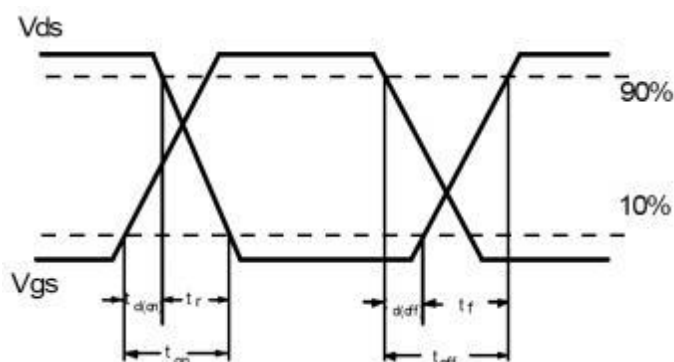
Electrical Characterizes @ $T_A=25C$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	60	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	65	90	m Ω	$V_{GS}=10V, I_D = 3A$
		—	80	120	m Ω	$V_{GS}=4.5V, I_D = 2A$
$V_{GS(th)}$	Gate threshold voltage	1	—	3	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source leakage current	—	—	10	μA	$V_{DS} = 60V, V_{GS} = 0V$
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 25V$
		—	—	-100		$V_{GS} = -25V$
Q_g	Total gate charge	—	7	—	nC	$I_D = 3A,$ $V_{DS}=48V,$ $V_{GS} = 4.5V$
Q_{gs}	Gate-to-Source charge	—	2	—		
Q_{gd}	Gate-to-Drain("Miller") charge	—	3	—		
$t_{d(on)}$	Turn-on delay time	—	6	—	ns	$V_{GS}=10V, V_{DS} = 30V,$ $R_{GEN}=3\Omega, I_D = 1A$
t_r	Rise time	—	5	—		
$t_{d(off)}$	Turn-Off delay time	—	16	—		
t_f	Fall time	—	3	—		
C_{iss}	Input capacitance	—	500	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1MHz$
C_{oss}	Output capacitance	—	50	—		
C_{rss}	Reverse transfer capacitance	—	40	—		

Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode) ①	—	—	3.5	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	20	A	
V_{SD}	Diode Forward Voltage	—	—	1.2	V	$I_S=1.7A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	—	27	—	ns	$T_J = 25^\circ C, I_F = 4A,$ $di/dt = 100A/\mu s$
Q_{rr}	Reverse Recovery Charge	—	32	—	nC	

Test Circuits and Waveforms

EAS Test Circuit:

Gate Charge Test Circuit:

Switching Time Test Circuit:

Switching Waveforms:


Notes:

- ① Calculated continuous current based on maximum allowable junction temperature.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$

Typical Electrical and Thermal Characteristics

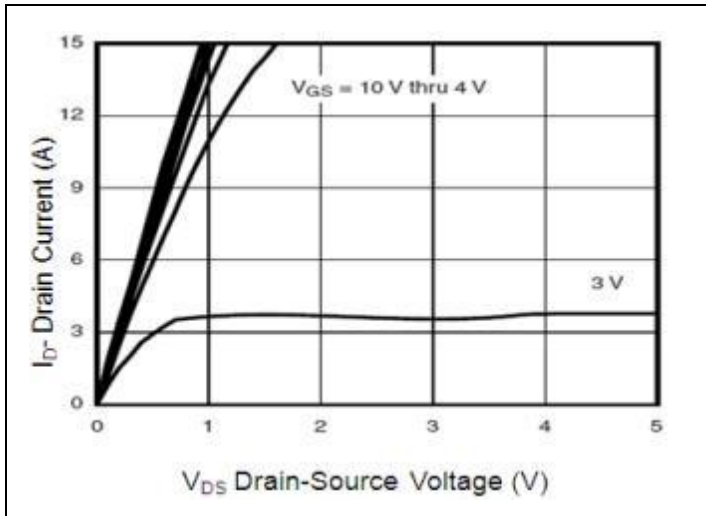


Figure1. Typical Output Characteristics

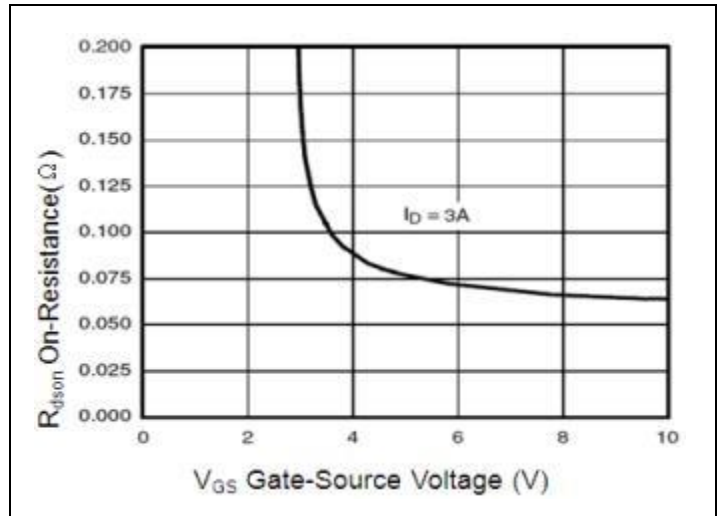


Figure2. Rds(on) vs. VGS

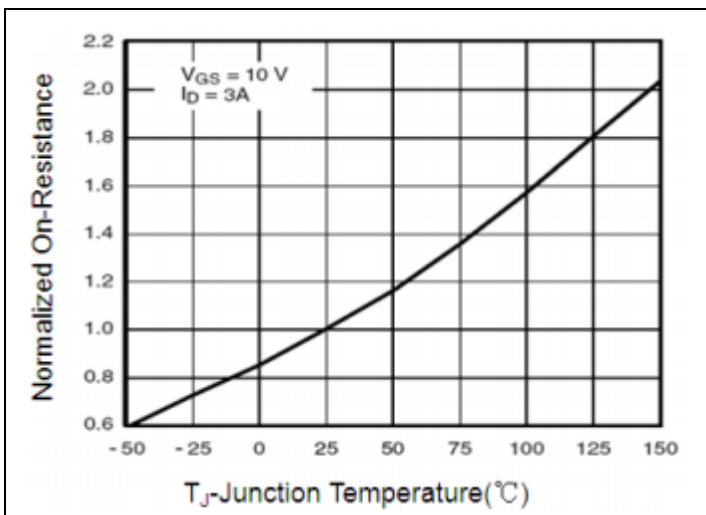


Figure3. Normalized On-Resistance vs. Junction Temperature

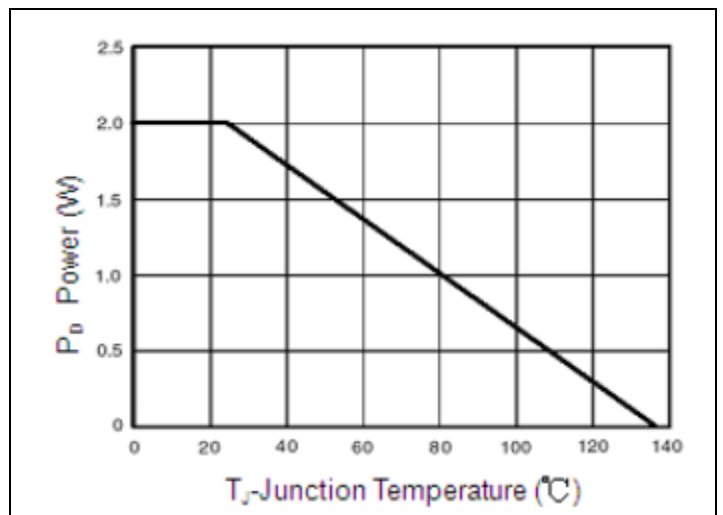


Figure4. Power Dissipation

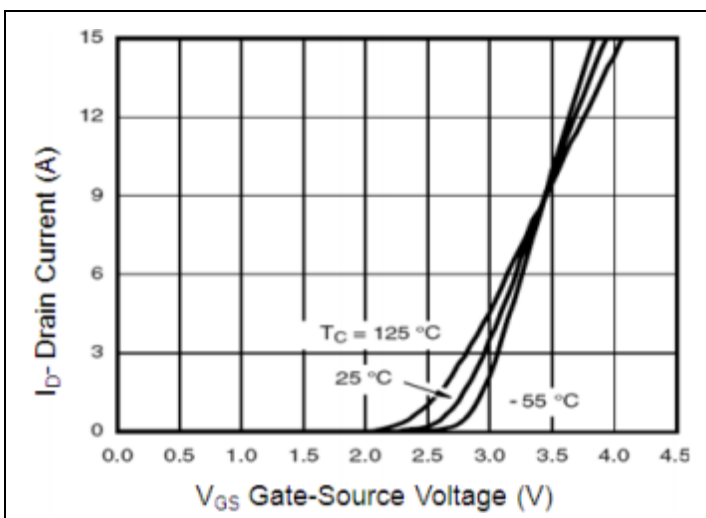


Figure5. Transfer Characteristics

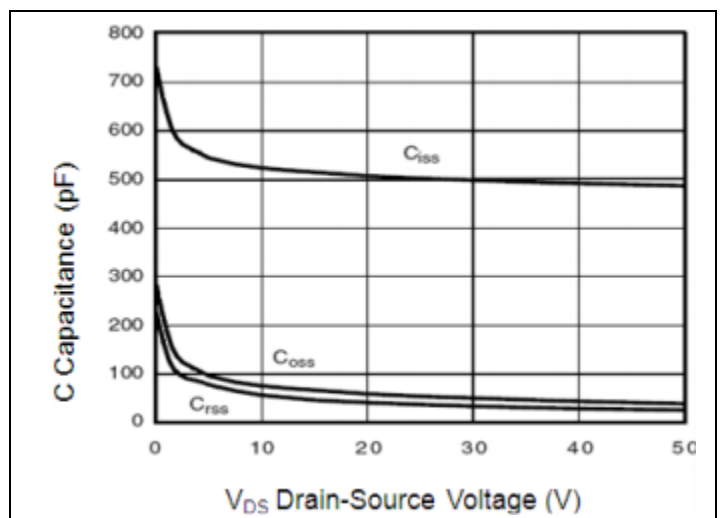


Figure6. Capacitance Characteristics

Typical Electrical and Thermal Characteristics

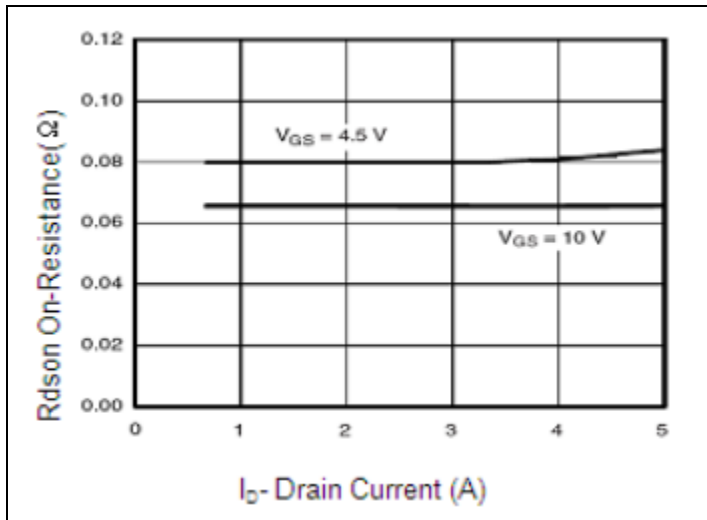


Figure7 . Drain Current vs. On-Resistance

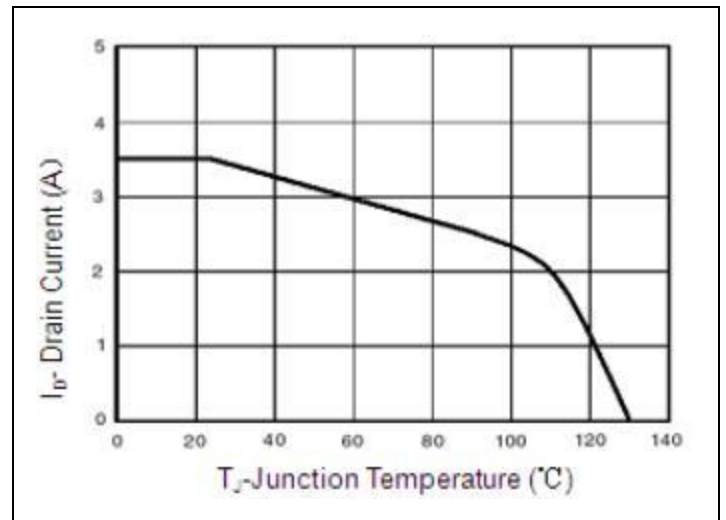


Figure8. Drain Current

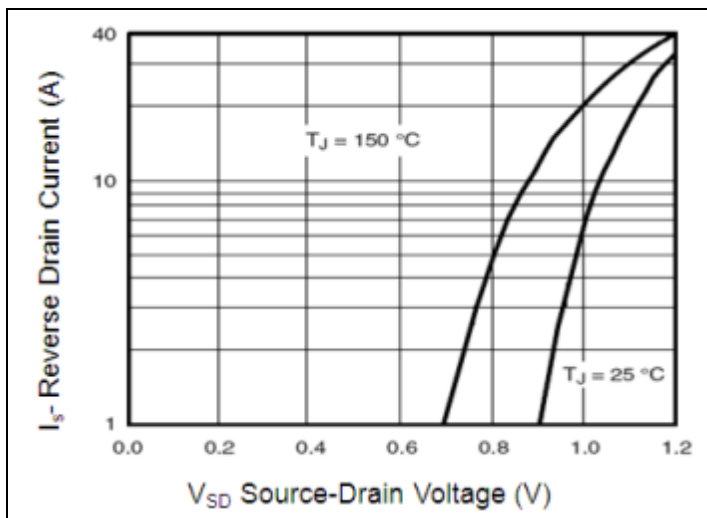


Figure9. Source-Drain Diode Forward

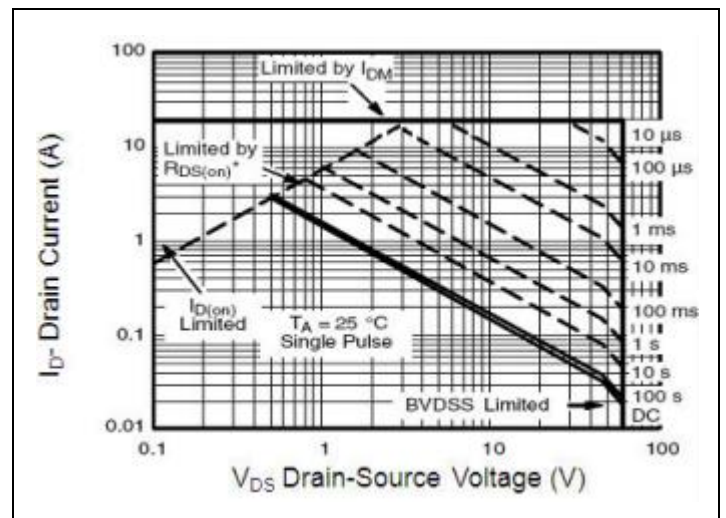


Figure10. Safe Operation Area

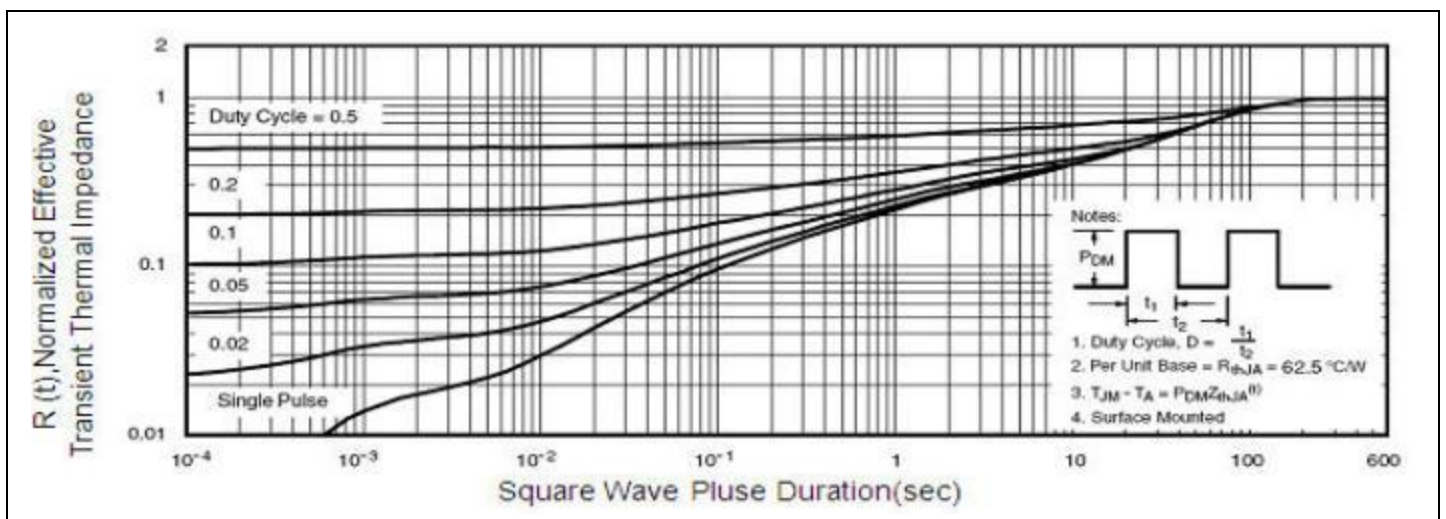
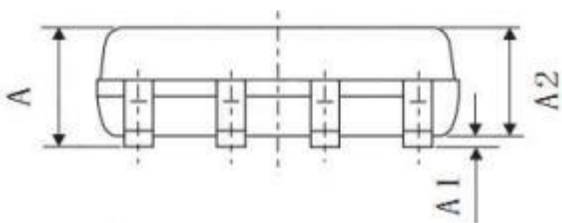
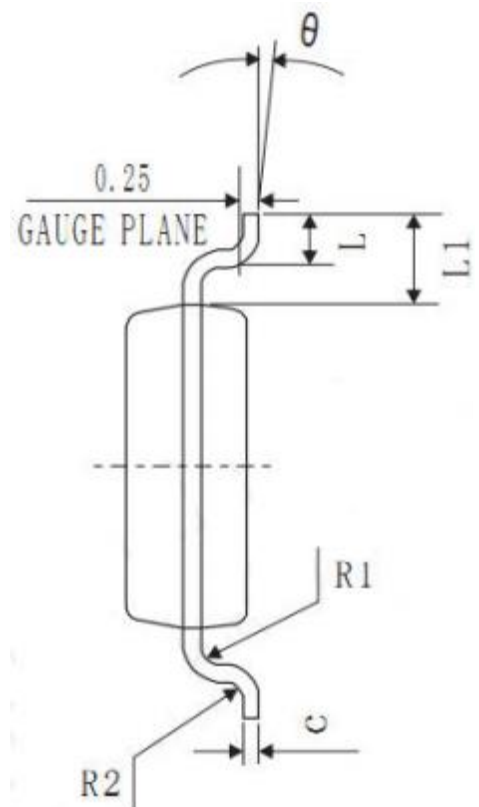
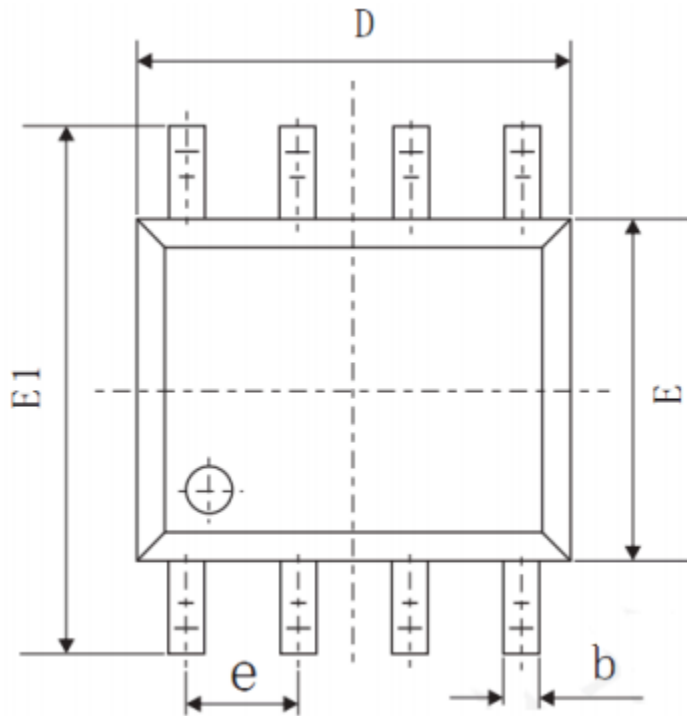


Figure 11. Normalized Maximum Transient Thermal Impedance

Mechanical Data:

Option 1

SOP-8 Package Outline (Unit: mm)

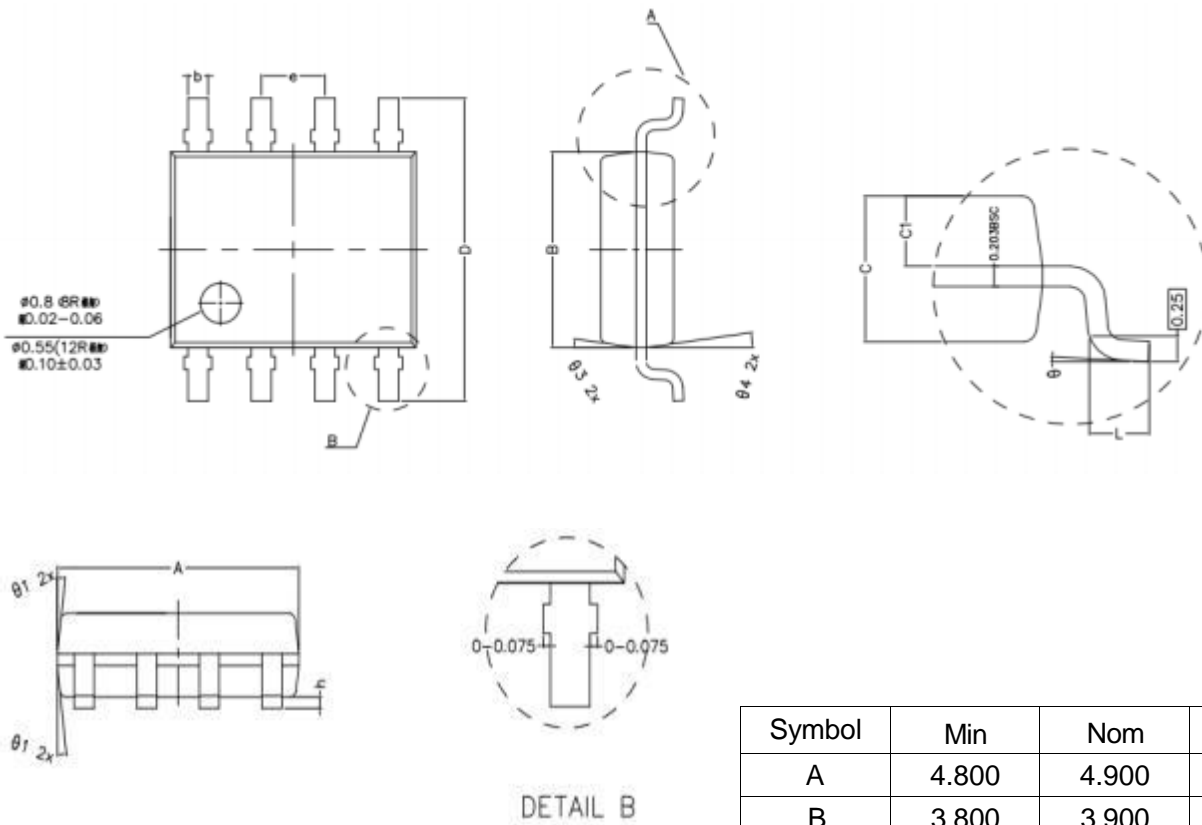


Symbol	Min	Nom	Max
A	1.40	1.60	1.80
A1	0.05	0.15	0.25
A2	1.35	1.45	1.55
b	0.30	0.40	0.50
c	0.153	0.203	0.253
D	4.80	4.90	5.00
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
L	0.45	0.70	1.00
theta	2°	4°	6°
L1	1.04REF		
e	1.27REF		
R1	0.07 REF		
R2	0.07 REF		

Mechanical Data:

Option 2

SOP-8 Package Outline (Unit: mm)



Symbol	Min	Nom	Max
A	4.800	4.900	5.000
B	3.800	3.900	4.000
C	1.350	1.450	1.550
C1	0.650	0.700	0.750
D	5.840	6.040	6.240
L	0.400	0.600	0.800
b	0.350	0.400	0.450
h	0.020	0.100	0.250
e	1.270TYPE		
$\theta 1$	7°TYPE(8R)	12°TYPE(12R)	
$\theta 2$	7°TYPE(8R)	10°TYPE(12R)	
$\theta 3$	8°TYPE(8R)	12°TYPE(12R)	
$\theta 4$	8°TYPE(8R)	10°TYPE(12R)	
θ	0°~8°		

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