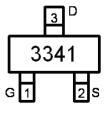
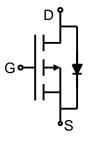


Main Product Characteristics:

V _{DSS}	-30V				
R _{DS} (on)	39mΩ (typ.)				
I _D	-4.2A ①				







SOT-23

Marking and Pin Assignments

Schematic Diagram

Features and Benefits:

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150°C operating temperature
- Add "HF" for Halogen Free



Description:

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute Max Rating: @T_A=25℃ unless otherwise specified

Symbol	Parameter	Max.	Units
I _D @ TC = 25°C	Continuous Drain Current, V _{GS} @ 10V ①	-4.2	
I _D @ TC = 70°C	Continuous Drain Current, V _{GS} @ 10V ①	-3.5	Α
I _{DM}	Pulsed Drain Current ②	-30	
P _D @TC = 25°C	Power Dissipation ③	1.4	W
V _{DS}	Drain-Source Voltage	-30	V
V _{GS}	Gate-to-Source Voltage	±12	V
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C

Thermal Resistance

Symbol	Characterizes	Тур.	Max.	Units
$R_{\theta JA}$	Junction-to-ambient (t ≤ 10s) ④	_	90	°C /W



Electrical Characterizes $@T_A=25^{\circ}C$ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions	
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	-30	_	_	V	$V_{GS} = 0V, I_D = -250\mu A$	
	Static Drain-to-Source on-resistance	_	39	50	mΩ	V _{GS} =-10V,I _D = -4.2A	
R _{DS(on)}		_	48	65		V _{GS} =-4.5V,I _D = -4A	
		_	68	120		V _{GS} =-2.5V,I _D = -1A	
V	Gate threshold voltage	-0.7	_	-1.3	V	$V_{DS} = V_{GS}, I_D = -250 \mu A$	
$V_{GS(th)}$	Gate threshold voltage	1	-0.68	_	V	T _J = 125°C	
I	Drain-to-Source leakage current	I	_	-1	μA	$V_{DS} = -24V, V_{GS} = 0V$	
I _{DSS}	Diam-to-Source leakage current	_	_	-50	μΑ	T _J = 125°C	
	Cata to Source forward lookage	_	_	100	nA	V _{GS} =12V	
I _{GSS}	Gate-to-Source forward leakage	_	_	-100		V _{GS} = -12V	
Qg	Total gate charge	_	18	_		$I_D = -4A$,	
Q _{gs}	Gate-to-Source charge	_	2.1	_	nC	V _{DS} =-25V,	
Q_{gd}	Gate-to-Drain("Miller") charge	-	2.7	_		V _{GS} = -10V	
t _{d(on)}	Turn-on delay time	-	7.5	_			
t _r	Rise time	_	15	_	no	V_{GS} =-10V, V_{DS} =-15V,	
$t_{\text{d(off)}}$	Turn-Off delay time	-	26	_	ns	R _{GEN} =3Ω	
t _f	Fall time		3.7	_			
C _{iss}	Input capacitance		712			$V_{GS} = 0V$,	
C _{oss}	Output capacitance		82		pF	V _{DS} =-15V,	
C _{rss}	Reverse transfer capacitance	_	67	_		f = 1MHz	

Source-Drain Ratings and Characteristics

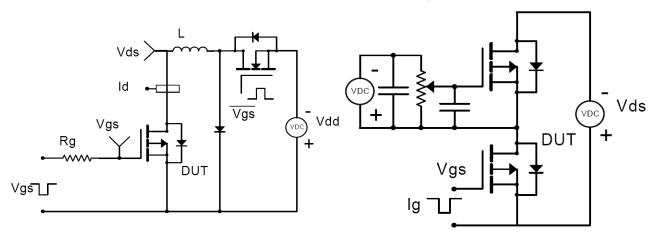
Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
Is	Continuous Source Current		_	-4.2	А	MOSFET symbol
	(Body Diode) ①					showing the
	Pulsed Source Current	_	_	-30	Α	integral reverse
I _{SM}	(Body Diode)					p-n junction diode.
V _{SD}	Diode Forward Voltage	_	-0.78	-1.0	V	I _S =-1A, V _{GS} =0V



Test Circuits and Waveforms

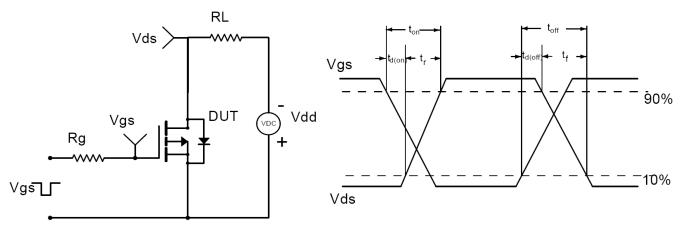
EAS Test Circuit:

Gate Charge Test Circuit:



Switching Time Test Circuit:

Switch Waveforms:

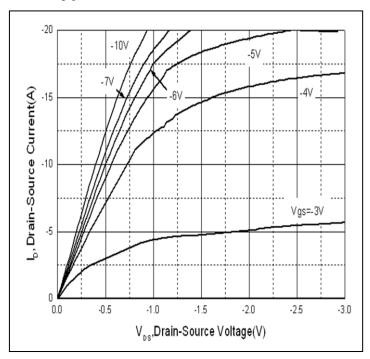


Notes:

- ①Calculated continuous current based on maximum allowable junction temperature.
- ②Repetitive rating; pulse width limited by max. junction temperature.
- ③The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- 4The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C



Typical Electrical and Thermal Characteristics



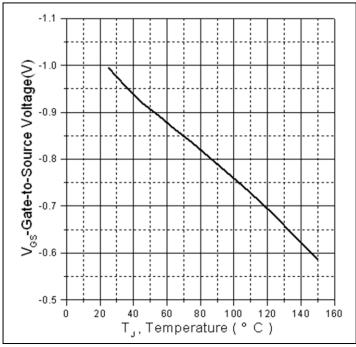
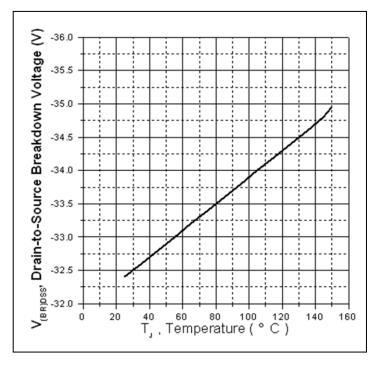


Figure 1. Typical Output Characteristics

Figure 2. Gate to Source Cut-off Voltage





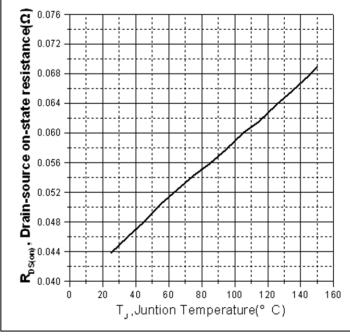
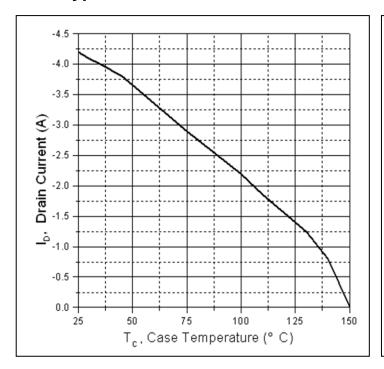


Figure 4. Normalized On-Resistance vs.

Junction Temperature



Typical Electrical and Thermal Characteristics



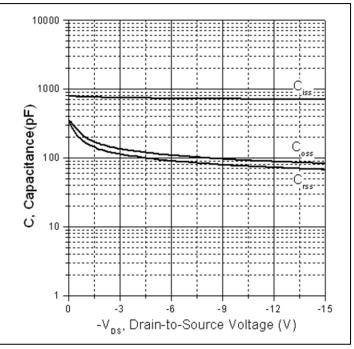


Figure 5. Maximum Drain Current vs. Case Temperature

Figure 6. Typical Capacitance vs. Drain-to-Source Voltage

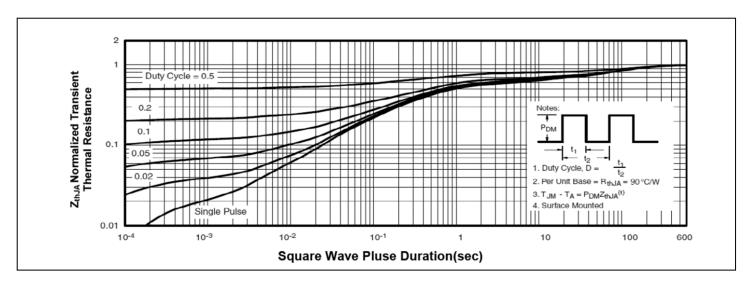
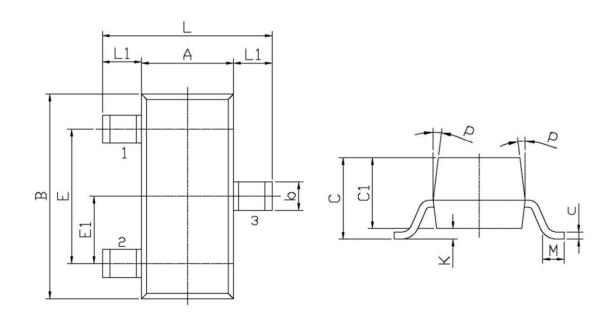


Figure 7. Maximum Effective Transient Thermal Impedance Junction-to-Case



Mechanical Data:



Symbol	Dimensions In Millimeters		6 1 1	Dimensions In Millimeters		
	Min	Max	Symbol	Min	Max	
L	2.2	2.7	С	1.30Ma×		
L1	0.45	0.65	C1	0.90	1.20	
Α	1.15	1.50	С	0.05	0.20	
В	2.70	3.10	К	0	0.10	
Ε	1.70	2.10	М	0.20MIN		
E1	0.85	1.05	Р	7°		
b	0.35	0,55				



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